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(71) Applicant: **MOTOROLA, INC.** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: **SUMMERS, Mark, David**; 4502 E. Grandview Rd., Phoenix, AZ 85232 (US). **HILL, Charles, Christopher**; 1465 N. Quail Lane, Gilbert, AZ 85233 (US). **CAMPINI, Edoardo**; 6951 E. Milagro Avenue, Mesa, AZ 85208 (US). **SILVERTHORN, Lee**; 5723 N. 33rd Place, Paradise Valley, AZ 85253 (US).

(74) Agents: **INGRASSIA, Vincent, B.** et al.; Motorola, Inc., P.O. Box 10219, Scottsdale, AZ 85271-0219 (US).

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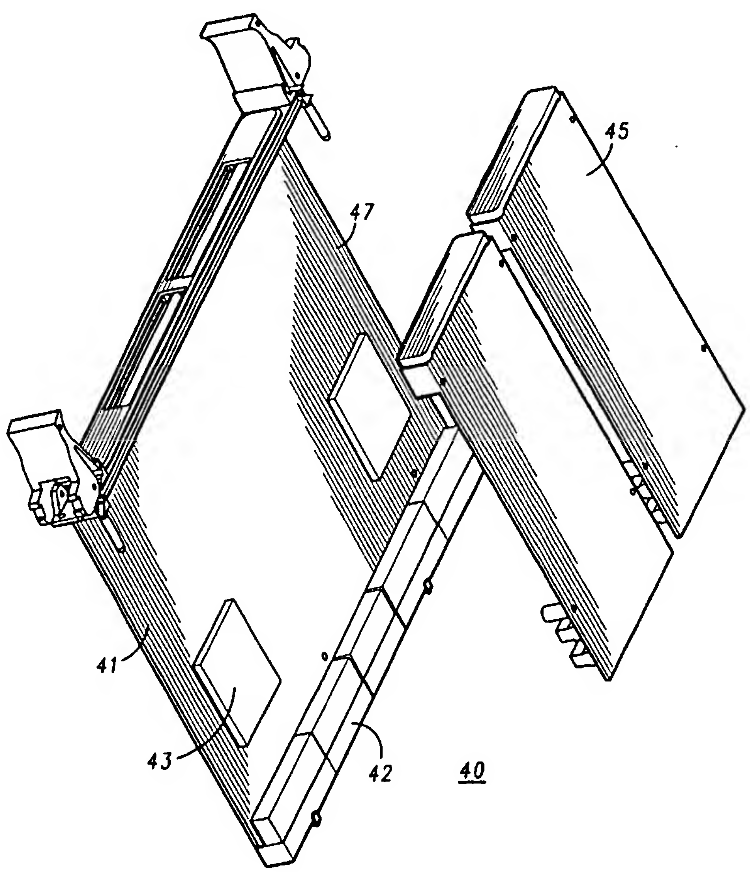
(54) Title: DUAL BRIDGE CARRIER CARD



(57) Abstract: A dual bridge carrier card (40) includes a first bridge circuit (47) mounted on the carrier card and connected to bridge a first bus in a first portion of a passive backplane (60) to a first extension bus in a second portion of the backplane (60). A second bridge circuit is mounted on the carrier card and connected to bridge a second bus in the first portion of the backplane (60) to a second extension bus in the carrier card. A plurality of PMC mounting positions are defined on the carrier card and connect the plurality of mounting positions to the second extension bus. The carrier card extends the backplane beyond the normal four slots (for PCI systems) and eight slots (for cPCI systems) and allows the mounting of PMCs on the same card.

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DUAL BRIDGE CARRIER CARD

Field of the Invention

This invention relates to apparatus and method for extending a passive backplane, and more particularly, to apparatus and method for extending a backplane beyond the normal number of loads.

Background of the Invention

Backplanes are used in computers, radios and many other types of equipment as a passive interconnect system. Previously, backplanes were specifically designed to prevent the passage of various signals, such as RF signals and the like, and were designed strictly as an interconnect for each individual card or load which was plugged into the backplane and to interconnect power to the various loads.

In the present technology, Peripheral Component Interconnect (PCI) backplanes are designed as a reflected wave local bus to carry various signals from a microprocessor or the like between the various loads. One drawback that is a result of this PCI reflected wave operation is a limitation on the number of cards or loads that can be installed in each backplane. For example, one type of backplane commonly referred to as a Peripheral Component Interconnect (PCI) is a reflected wave local bus that is limited to four loads. A newer system, commonly referred to as compact PCI (cPCI) can receive up to eight loads.

Originally, bridges were built into the backplane to create an active backplane and extend the backplane to allow the installation of more loads. This system has a complexity problem because of the active PCI bridge chips and circuitry built into the backplane. The bridge chips and the extra installation is expensive and is undesirable in many applications. A commercial two card and cable solution, such as the SBS BIT-3 extender cards, requires the use of two slots and also requires cable management. A rear I/O bridge design has been devised for extending a passive backplane but requires at least one rear mounted

card. This design is much less desirable because in many applications there is no room for traditional vertical rear I/O cards.

In each of the PCI and cPCI systems, if additional loads are required (beyond the original loads), the backplane must be extended either by active bridging in the backplane or by using a bridge card in a passive backplane. When using the two card and cable solution, the bridge cards must be installed as loads (in two of the slots) and they then serve as a source for an additional group of loads. Each bridge card extends the backplane by a number equal to the original number of loads, i.e. four loads in the PCI system and eight loads in the cPCI system. Bridge cards are a well known commercially available component and their use is well known.

The bridge cards have several problems that are highly undesirable. First, additional cabling is required to connect the two bridge cards. The cabling entails the usual cabling problems in addition to requiring additional room in the equipment. Generally, the cabling extends from an end of one of the bridge cards opposite the plug end to an end of the second adjacent bridge card. Thus, a cable loop is formed that requires additional room in the equipment case. In some instances the cable loop and bridge cards are in a rear mounted card positioned on the opposite side of the backplane, which means that the backplane can not be mounted directly on a chassis but must be spaced from the chassis to accommodate the bridge card and cable loop.

Further, the cable cards are plugged into the last load slot in the previous series of load slots (i.e. the fourth load slot in the PCI system and the eighth load slot in the cPCI system) and the first slot of the next series so that two less slots are available to use for load purposes. Thus, using the two card and cable solution in the PCI system results in space for a total of six loads and a total of fourteen loads in the cPCI system.

Accordingly it is highly desirable to provide apparatus and/or a method of eliminating or reducing these problems.

Brief Description of the Drawings

Referring to the drawings:

FIG. 1 is a simplified side elevational view of an active backplane;

FIG. 2 is a simplified side elevational view of a prior art dual bridge and cable backplane extension;

FIG. 3 is a simplified side elevational view of a prior art rear mounted backplane extension;

FIG. 4 is an exploded isometric view of a dual bridge carrier card in accordance with the present invention;

FIG. 5 is a simplified block diagram of the dual bridge carrier card illustrated in FIG. 4, showing the various connections; and

FIG. 6 is a simplified block diagram of a backplane constructed to receive and be extended by the dual bridge carrier card of FIG. 1.

Description of the Preferred Embodiment

Turning now to the figures, FIG. 1 is a simplified side elevational view of an active PCI backplane 10 with a first plurality of slots 11 positioned on an upper surface thereof. In this specific example, active PCI backplane 10 includes four slots 11. An active PCI bridge chip 12 and associated circuitry is built into backplane 10 to extend backplane 10 and provide for extended slots 14 to allow for the installation of more loads. However, the bridge chips and the extra installation are expensive and are not used in many applications. Thus, the active backplane must either be fabricated in a variety of different embodiments (i.e. not extended mode. extended mode, etc.) or some of the smaller embodiments will be very expensive.

Turning now to FIG. 2, a simplified side elevational view of a prior art dual bridge and cable PCI backplane extension apparatus, generally designated 15, is illustrated. PCI backplane extension apparatus 15 includes a backplane 16 having a plurality (four in this example) of slots 17 positioned on the upper surface thereof. An extension PCI backplane 18, having a plurality of slots 19 on the

upper surface thereof, is positioned adjacent to backplane 16. A first bridge card 20 having a bridge 21 mounted thereon is inserted into the final slot 17 on backplane 16. A second bridge card 22 having a bridge 23 mounted thereon is inserted into the first slot 19 on extension backplane 18. Cabling 24 is installed to actively connect bridge card 20 to bridge card 22.

Thus, the bridge cards 20 and 22 are installed as loads and they serve as a source for extension PCI backplane 18. Bridge cards 20 and 22 extend the backplane by a number equal to the original number of loads, i.e. four loads in the PCI system and eight loads in the cPCI system. The problem is that the commercial two card and cable solution, such as the SBS BIT-3 extender cards, requires the use of two slots and also requires cable management. Bridge cards 20 and 22 have several problems that are highly undesirable. First, additional cabling 24 is required to connect bridge cards 20 and 22. The cabling entails the usual cabling problems in addition to requiring additional room in the equipment. Generally, the cabling extends from an upper end of bridge card 20 opposite the plug end to an upper end of bridge card 22. Thus, a cable loop is formed that requires additional room in the equipment case. Also, bridge cards 20 and 22 are plugged into the last slot 17 in backplane 16 (i.e. the fourth slot in the PCI system and the eighth slot in the cPCI system) and the first slot 19 of extension backplane 18 so that two less slots are available to use for load purposes. Thus, using the two card and cable solution in the PCI system results in space for a total of six loads and a total of fourteen loads in the cPCI system.

Referring to FIG. 3, a simplified side elevational view of prior art rear mounted PCI backplane extension apparatus, generally designated 25, is illustrated. PCI backplane extension apparatus 25 includes a backplane 26 having a plurality (four in this example) of slots 27 positioned on the upper surface thereof. An extension PCI backplane 28, having a plurality of slots 29 on the upper surface thereof, is positioned adjacent to backplane 26. A first bridge card 30 having a bridge 31 mounted thereon is affixed to the rear surface of backplane 26. A second bridge card 32 having a bridge 33 mounted thereon is affixed to the rear surface of extension backplane 28. Cabling 34 is installed to actively connect bridge card 30 to bridge card 32. The rear I/O bridge design has been devised for

extending a passive PCI backplane but requires the rear mounted cards. This design is much less desirable because in many applications there is no room for traditional vertical rear I/O cards. For rear mounted cable loop and bridge cards positioned on the opposite side of the backplane, the backplane can not be mounted directly on a chassis but must be spaced from the chassis to accommodate the bridge cards and cable loop.

Turning now to FIG. 4 an isometric view is illustrated of a dual bridge carrier card 40 in accordance with the present invention. FIG. 5 is a simplified block diagram of dual bridge carrier card 40, showing the various connections. Dual bridge carrier card 40 is designed for use in a passive backplane and includes a supporting substrate and interconnect 41, which may be a standard printed circuit board or the like, and includes circuitry for interconnecting and powering the various components mounted thereon. Supporting substrate and interconnect 41 also includes a plurality of multi-pin connection jacks, generally designated 42, positioned along one edge for engagement in mating plugs in a passive backplane. As is understood in the art and referring to FIG. 5, this preferred embodiment includes five standard connection jacks J1 through J5.

Referring additionally to FIG. 6, a simplified block diagram is illustrated of a passive backplane 60 constructed to receive and be extended by dual bridge carrier card 40. In this preferred embodiment, backplane 60 embodies a compact Peripheral Component Interconnect (cPCI) system, which can support as many as eight individual cards or loads without extension, but it could also be used in a Peripheral Component Interconnect (PCI) system as is used, for example, in commercial personal computers. Further, while specific connection jacks and mating plugs are described in conjunction with this preferred embodiment, it will be understood by those skilled in the art that backplanes are normally wired special by the user and connection jacks and mating plugs other than those described below can be used.

Passive backplane 60 includes a plurality of carrier card receiving slots, designated slot 1 through slot 12 in FIG. 6, with slot 1 through slot 5 being representatively illustrated. Each of the plurality of carrier card receiving slots includes five plugs, designated P1 through P5, formed to mate with connection

jacks J1 through J5 of carrier cards, such as carrier card 40. As will be understood by the skilled artisan, passive backplane 60 is wired, generally specifically for a designated user. In this embodiment, backplane 60 includes a first signal bus 61, which is wired into plug P1 and P2 of slots 1 - 7 and is limited to only plug P1 of slot 8. In a normal fashion, a power bus 62 is associated with and extends parallel to signal bus 61. A second signal bus 63 is wired into plug P4 of slot 7 and extends to plug P5 of slot 8. In a normal fashion, a power bus 64 is associated with and extends parallel to signal bus 63. Slot 9 through slot 12 and any additional slots of backplane 60 are wired so that an extension signal bus 65 and extension power bus 66 are wired into plug P4 of each slot. Also, a separate signal bus 67 is wired into each plug P1 and P2 of slot 9 through slot 12 and any additional slots of backplane 60 and a power bus 68 is associated with and extends parallel to signal bus 67.

Referring again to FIG. 5, a bridge circuit 43 is mounted on supporting substrate and interconnect 41 of card 40 so as to bridge a signal bus 43, which is wired into connection jack J5, with a signal bus 46, which is wired into connection jack J4. Referring additionally to FIG. 6, it can be seen that signal bus 43 connects to signal bus 63 and signal bus 46 connects to extension signal bus 65 when card 40 is plugged into slot 8 of backplane 60. Further, associated power buses 64 and 66 are interconnected by card 40 in a well known fashion, which is not shown or explained to simplify this disclosure.

A bridge circuit 47 is mounted on supporting substrate and interconnect 41 of card 40 so as to bridge a signal bus 48, which is wired into connection jack J1, with an extension signal bus 49, which is wired into passive backplane 41 of card 40. Extension signal bus 49 provides a plurality of general purpose module mounting positions for mounting a plurality of PCI Mezzanine Card (PMC) modules 45 or the like, sometimes referred to as daughter modules or cards, on supporting substrate and interconnect 41 of card 40. Signal outputs for modules 45 are connected to connection jacks J2 and J3 in a well known fashion and will not be elaborated upon herein. Referring additionally to FIG. 5, it can be seen that signal bus 48 connects to signal bus 61 when card 40 is plugged into slot 8 of backplane 60. Further, associated power bus 62 is interconnected to card 40 in a

well known fashion, which is not shown or explained to simplify this disclosure. Thus, bridge 43 connects signal bus 48, which is connected to signal bus 61, to extension signal bus 49, thereby connecting the plurality of general purpose module mounting positions 45 and extension signal bus 49 to signal bus 61.

Thus, dual bridge carrier card 40 extends passive backplane 60 to more than eight carrier card receiving slots and does not require the use of one or more of the eight slots and/or extensions for mounting purposes, since a plurality of general purpose modules 45 can be mounted on dual bridge carrier card 40. Further, dual bridge carrier card 40 can be simply plugged into backplane 60 to extend backplane 60 an additional number of carrier card receiving slots, so that major modifications of the backplane are not required and the extension can be made or removed with little or no extra cost and modifications.

While we have shown and described specific embodiments of the present invention, further modifications and improvements will occur to those skilled in the art. We desire it to be understood, therefore, that this invention is not limited to the particular forms shown and we intend in the appended claims to cover all modifications that do not depart from the spirit and scope of this invention.

CLAIMS

What is claimed is:

1. A dual bridge carrier card for use in a passive backplane comprising:

a first bridge circuit mounted on a carrier card and connected to bridge a first bus in a first portion of a passive backplane to a first extension bus in a second portion of the passive backplane;

a second bridge circuit mounted on the carrier card and connected to bridge a second bus in the first portion of the passive backplane to a second extension bus in the carrier card; and

a plurality of general purpose module mounting positions defined on the carrier card and connecting the plurality of general purpose module mounting positions to the second extension bus.

2. A dual bridge carrier card for use in a passive backplane as claimed in claim 1 wherein the carrier card and passive backplane are incorporated into one of a Peripheral Component Interconnect (PCI) system and a compact PCI system.

3. A dual bridge carrier card for use in a passive backplane comprising:

a supporting substrate and interconnect including a plurality of multi-pin connection jacks positioned along one edge for engagement in mating plugs in a passive backplane, a first of the plurality of multi-pin connection jacks being connected to engage a first bus in the passive backplane, a second of the plurality of multi-pin connection jacks being connected to engage a second bus in a first portion of the passive backplane, a third of the plurality of multi-pin connection jacks being connected to engage a second extension bus in a second portion of the passive backplane, and ;

first and second bridge circuits mounted on the supporting substrate, the first bridge circuit connected to the first of the plurality of multi-pin connection jacks and bridging the first bus in the passive backplane to a first extension bus in the supporting substrate and interconnect and the second bridge circuit connected to

the second and third of the plurality of multi-pin connection jacks and bridging between the second bus in the first portion of the passive backplane and the second extension bus in the second portion of the passive backplane; and

a plurality of general purpose module mounting positions defined on the supporting substrate and connecting the plurality of general purpose module mounting positions to the first extension bus.

4. A dual bridge carrier card for use in a passive backplane as claimed in claim 3 wherein the carrier card and passive backplane are incorporated into a Peripheral Component Interconnect (PCI) system.

5. A dual bridge carrier card for use in a passive backplane as claimed in claim 3 wherein the carrier card and passive backplane are incorporated into a compact Peripheral Component Interconnect (cPCI) system.

6. A dual bridge carrier card for use in a passive backplane as claimed in claim 5 wherein the plurality of general purpose module mounting positions are designed to receive PCI Mezzanine Cards (PMC) therein.

7. A dual bridge carrier card for use in a passive backplane comprising:

a passive backplane having first and second buses in a first portion and first and second extension buses in a second portion, the passive backplane defining a plurality of carrier card receiving slots in the first and second portions and each slot including a plurality of plugs, a first carrier card receiving slot of the plurality of carrier card receiving slots including a first plug electrically connected to the first bus, a second plug electrically connected to the first extension bus, and a third plug electrically connected to the second bus;

a bridging carrier card including a supporting substrate and interconnect with a plurality of multi-pin connection jacks positioned along one edge for engagement in mating plugs in the passive backplane, the bridging carrier card being positioned in the first carrier card receiving slot of the passive backplane with a first jack of the plurality of multi-pin connection jacks being engaged in the

first plug of the passive backplane, a second jack of the plurality of multi-pin connection jacks being engaged in the second plug of the passive backplane, and a third jack of the plurality of multi-pin connection jacks being engaged in a third plug of the passive backplane;

first and second bridge circuits mounted on the supporting substrate, the first bridge circuit connected to the first jack of the plurality of multi-pin connection jacks and bridging the first bus in the passive backplane to a first extension bus in the supporting substrate and interconnect, and the second bridge circuit connected to the second and third jacks of the plurality of multi-pin connection jacks and bridging between the second bus in the first portion of the passive backplane and the second extension bus in the second portion of the passive backplane; and

a plurality of general purpose module mounting positions defined on the supporting substrate and connecting the plurality of general purpose module mounting positions to the second extension bus.

8. A dual bridge carrier card for use in a passive backplane as claimed in claim 7 wherein the carrier card and passive backplane are incorporated into a Peripheral Component Interconnect (PCI) system.

9. A dual bridge carrier card for use in a passive backplane as claimed in claim 7 wherein the first carrier card receiving slot is a fourth slot of the plurality of carrier card receiving slots.

10. A dual bridge carrier card for use in a passive backplane as claimed in claim 8 wherein the plurality of plugs in the passive backplane include plug P1, plug P2, plug P3, plug P4 and plug P5, and the first plug electrically connected to the first bus is plug P5, the second plug electrically connected to the first extension bus is plug P4, and the third plug electrically connected to the second bus is plug P1.

11. A dual bridge carrier card for use in a passive backplane as claimed in claim 7 wherein the carrier card and passive backplane are incorporated into a compact Peripheral Component Interconnect (cPCI) system.

12. A dual bridge carrier card for use in a passive backplane as claimed in claim 11 wherein the first carrier card receiving slot is an eighth slot of the plurality of carrier card receiving slots.

13. A dual bridge carrier card for use in a passive backplane as claimed in claim 11 wherein the plurality of plugs in the passive backplane include plug P1, plug P2, plug P3, plug P4 and plug P5, and the first plug electrically connected to the first bus is plug P5, the second plug electrically connected to the first extension bus is plug P4, and the third plug electrically connected to the second bus is plug P1.

14. A dual bridge carrier card for use in a passive backplane as claimed in claim 11 wherein the plurality of general purpose module mounting positions are designed to receive PCI Mezzanine Cards (PMC) therein.

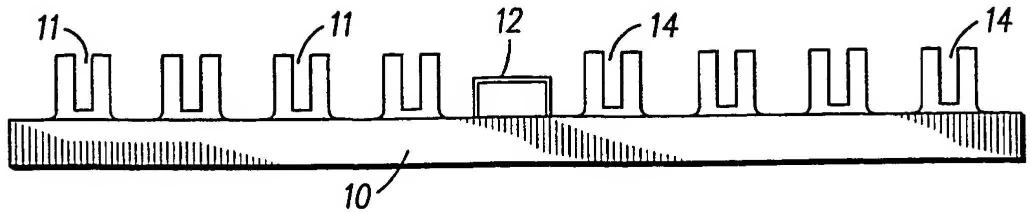
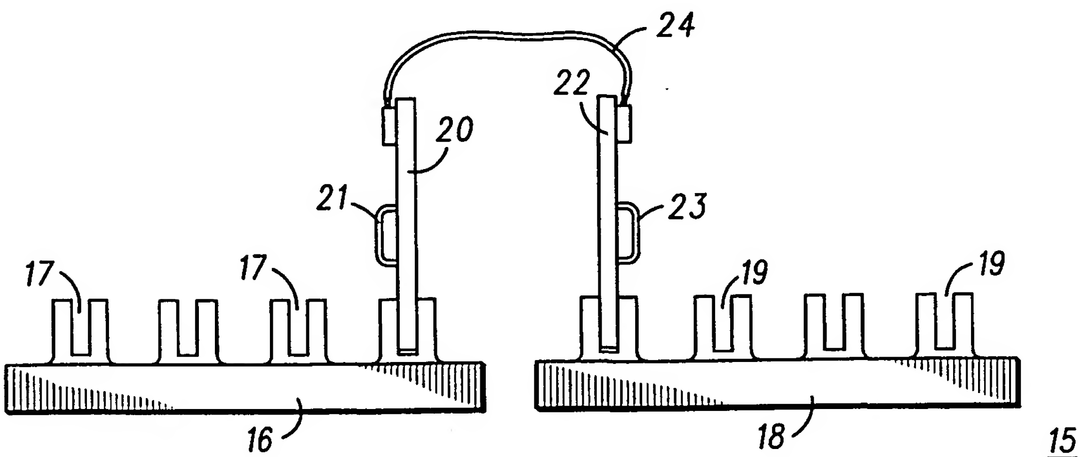
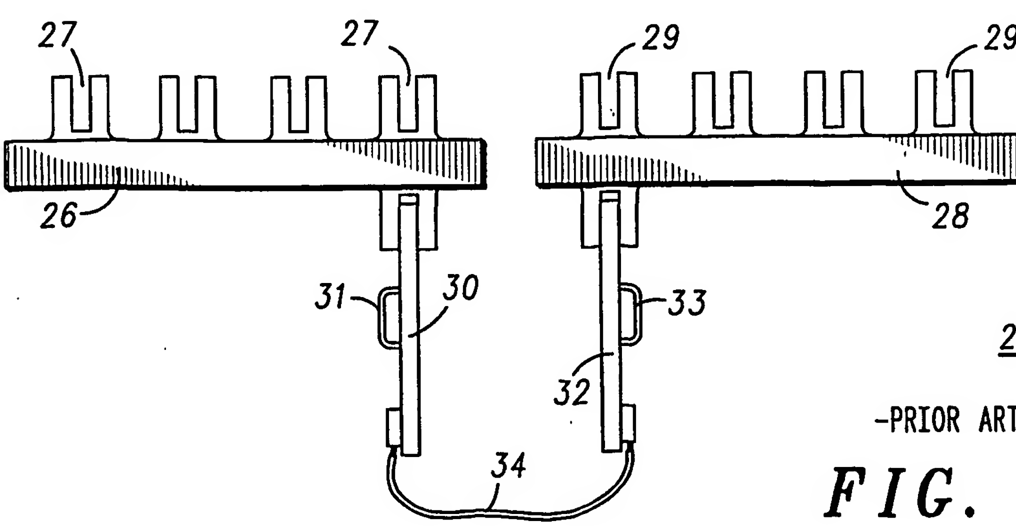


FIG. 1



-PRIOR ART-

FIG. 2



-PRIOR ART-

FIG. 3

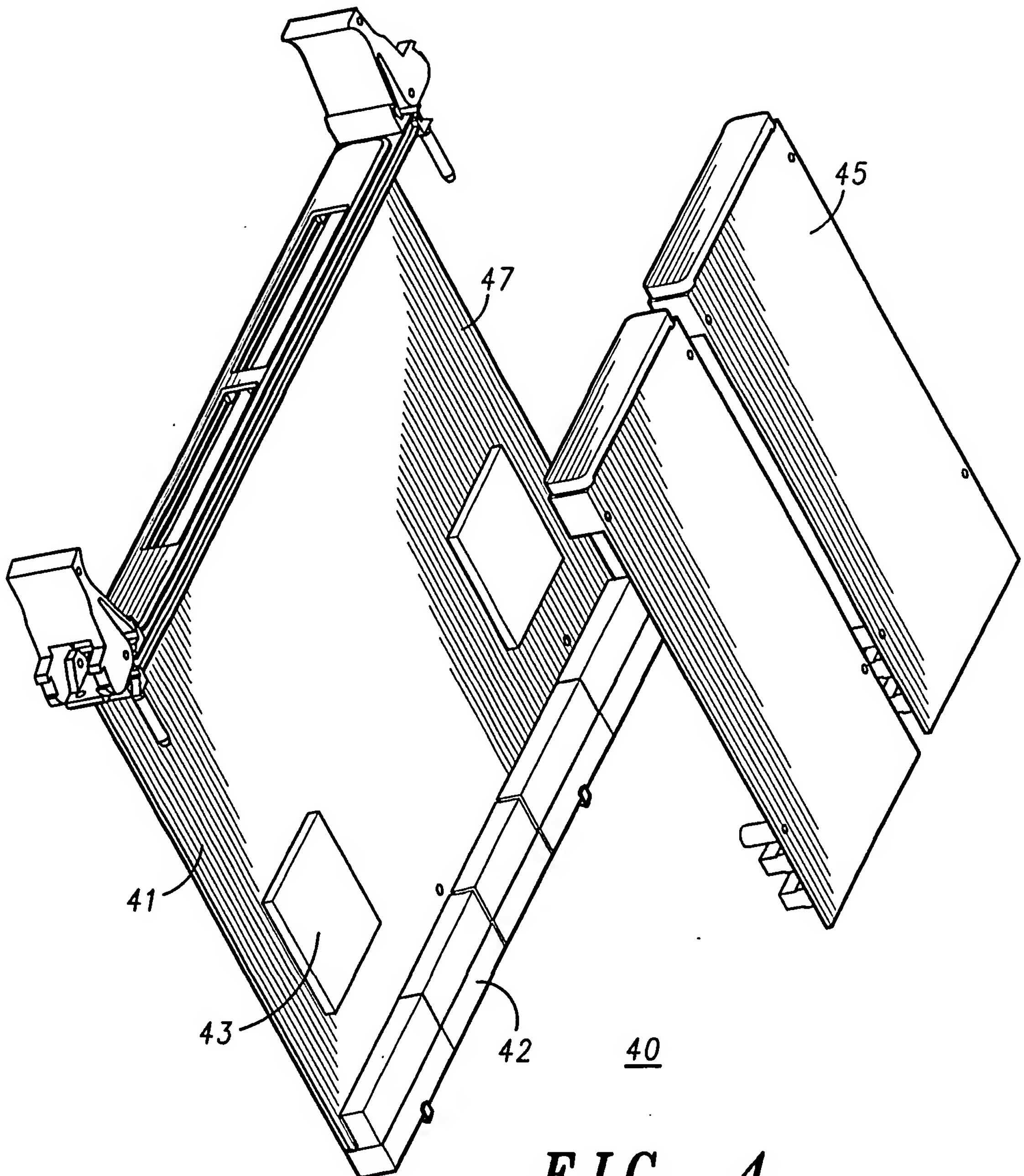


FIG. 4

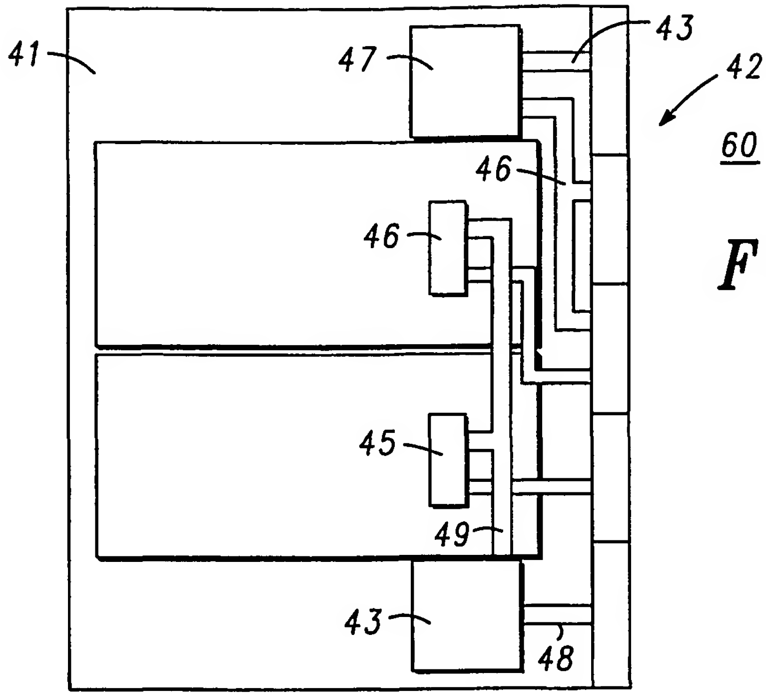
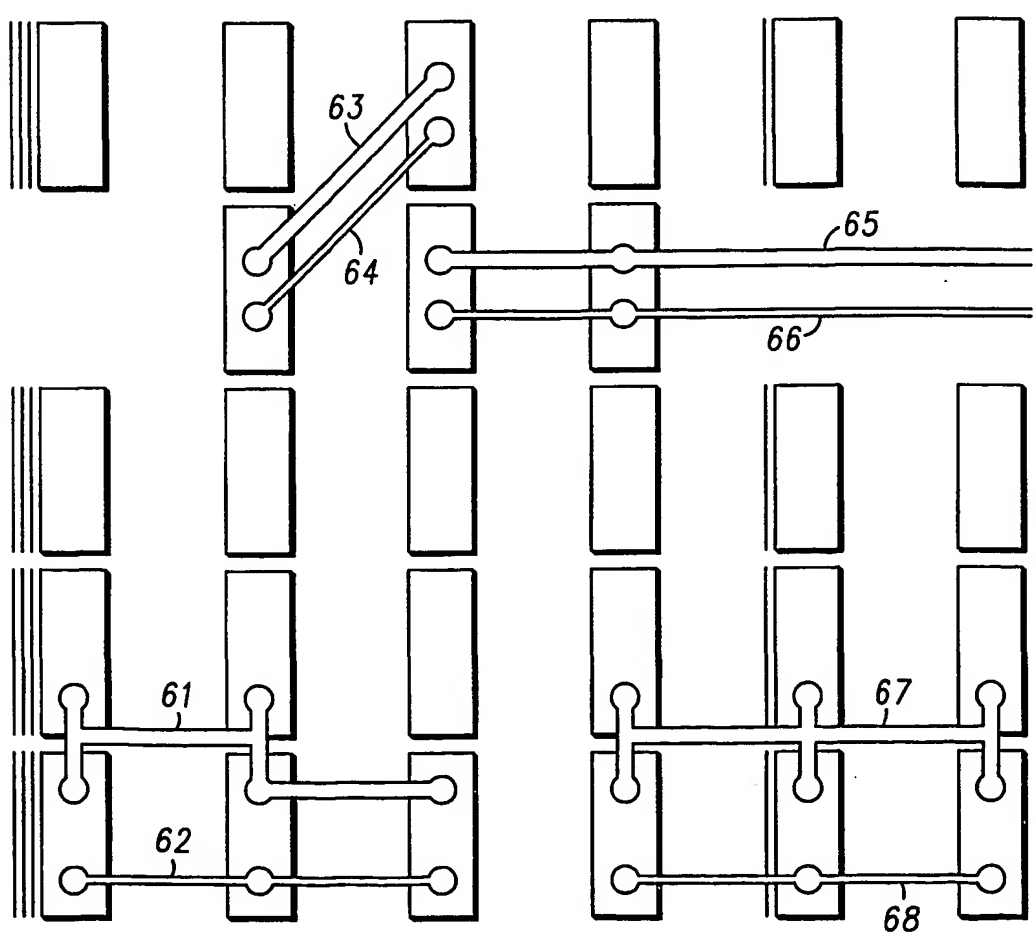


FIG. 5

FIG. 6

60



INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F13/40 H05K7/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F H05K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 59075 A (MOTOROLA INC) 18 November 1999 (1999-11-18) the whole document	1,3,7
A	US 5 754 796 A (WANG DANIEL ET AL) 19 May 1998 (1998-05-19) the whole document	1,3,7
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A	US 5 793 998 A (COPELAND JEFFREY P ET AL) 11 August 1998 (1998-08-11) the whole document	6,14

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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11 May 2001	18/05/2001

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte ...onal Application No
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